

Reblewski -- 10/824,489
Atty. Docket No.: 003921.00008

REMARKS

This paper is responsive to the final Office Action mailed July 31, 2008. Reconsideration and allowance are respectfully requested. No new matter is added by this Amendment. Claim 3 has been canceled. Claims 1, 2, and 4-10 remain pending. Claim 3 has been canceled without prejudice or disclaimer. Claims 1, 4, 6, and 8 have been amended. New claims 15-24 have been added. No new matter has been introduced.

Claims 1, 2, and 4-10 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,907,697 to Barbier, et al. (Barbier II), which is a CIP of previously asserted U.S. Patent No. 5,574,388 to Barbier, et al. (Barbier I). Claim 3 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Barbier II in view of alleged common knowledge. Applicant respectfully traverses these rejections in view of the amendments and remarks herein.

Independent Claims 1, 4, 6, and 8

Independent Claims 1, 4, 6, and 8 have been amended to include some of the features of canceled claim 3. Specifically, the following feature has been added to each of these claims.

“memory, wherein the reconfigurable interconnect network is configured to dynamically re-configure the first, second, and third reconfigurable interconnect stages in accordance with a content of the memory.”

The Action asserts in paragraph 8 (and in previous office actions) that Barbier II (and Barbier I) teach an interconnect stage “being dynamically configured in accordance with a content of the memory.” Applicant respectfully asserts that the office action misinterprets Barbier I and II. Both Barbier I and II disclose a single “memory 112.” (Figure 3). Barbier I and II specifically state that “[m]emory 112 facilitates usage of [special purpose] FPGA 100 to emulate circuit design with memory elements.” (Barbier I, column 4, lines 43-44; Barbier II, column 4, lines 59-61)(emphasis added). Barbier I and Barbier II do not disclose any other use of “memory 112.” Accordingly, “memory 112” is used for modeling “memory,” not for configuring interconnects.

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For at least this reason, Applicant submits that amended independent claim 1, 4, 6, and 8 distinguishes over the references of record, and is in condition for allowance.

Dependent Claims

The dependent claim 2, 5, 7, and 9-11 are also believed allowable by virtue of depending from allowable independent claims, and further in view of the additional features recited therein.

New Claims

New claims 15-17 recites similar features as discussed above, and thus are believed to be allowable for at least the same reasons discussed. New claims 18-24 recite various other features already disclosed in the specification that are not disclosed in the art of record. Therefore, Applicant believes these claims to also be allowable.

Conclusion

All rejections having been addressed, it is submitted that the present application is in condition for allowance, and notice to that effect is respectfully requested. Should the Examiner have any questions, the Examiner is invited to contact the undersigned at the number below.

Respectfully submitted,

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